NCS7101

1.8 Volt Rail-to-Rail Operational Amplifier

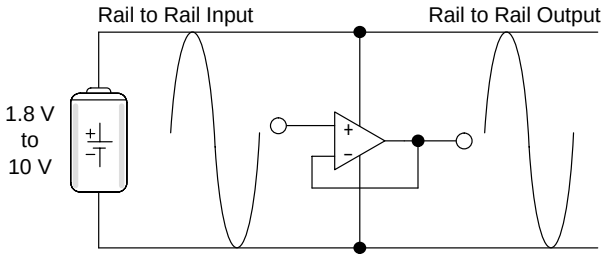
The NCS7101 operational amplifier provides rail−to−rail operation on both the input and output. The output can swing within 50 mV of each rail. This rail−to−rail operation enables the user to make full use of the entire supply voltage range available. It is designed to work at very low supply voltages (1.8 V and ground), yet can operate with a supply of up to 10 V and ground. The NCS7101 is available in the space saving SOT−23−5 package with two industry standard pinouts.

Features

- Low Voltage, Single Supply Operation (1.8 V and Ground to 10 V and Ground)
- 1.0 pA Input Bias Current
- Unity Gain Bandwidth of 1.0 MHz at 5.0 V, 0.9 MHz at 1.8 V
- Output Voltage Swings Within 50 mV of Both Rails @ 1.8 V
- No Phase Reversal on the Output for Over−Driven Input Signals
- Input Offset Trimmed to 1.0 mV
- Low Supply Current (I_D = 1.0 mA)
- Works Down to Two Discharged NiCd Battery Cells
- ESD Protected Inputs Up to 2.0 kV
- Pb−Free Package is Available

Typical Applications

- Dual NiCd/NiMH Cell Powered Systems
- Portable Communication Devices
- Low Voltage Active Filters
- Power Supply Monitor and Control
- Interface to DSP



This device contains 68 active transistors.

Figure 1. Typical Application

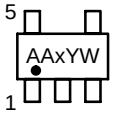
ON Semiconductor®

http://onsemi.com

LOW VOLTAGE RAIL−TO−RAIL OPERATIONAL AMPLIFIER

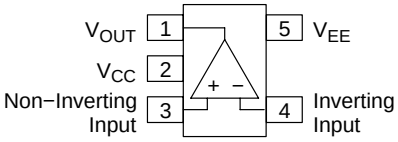
CASE 483
SOT−23−5
SN SUFFIX

MARKING DIAGRAM

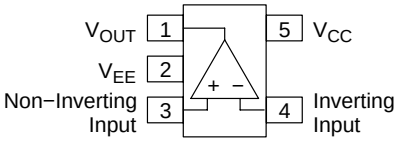


x = C for SN1
D for SN2
Y = Year
W = Work Week

PIN CONNECTIONS



Style 1 Pin Out (SN1T1)



Style 2 Pin Out (SN2T1)

ORDERING INFORMATION

Device	Package	Shipping†
NCS7101SN1T1	SOT−23−5	3000 Tape & Reel (7 inch Reel)
NCS7101SN1T1G	SOT−23−5 (Pb−Free)	
NCS7101SN2T1	SOT−23−5	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	10	V
Input Differential Voltage Range (Note 1)	V_{IDR}	V_{EE} − 300 mV to 10 V	V
Input Common Mode Voltage Range (Note 1)	V_{ICR}	V_{EE} − 300 mV to 10 V	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Junction Temperature	T_J	150	°C
Power Dissipation and Thermal Characteristics SOT−23−5 Package Thermal Resistance, Junction−to−Air Power Dissipation @ T_A = 70°C	 $R_{\theta JA}$ P_D	 220 364	 °C/W mW
Storage Temperature Range	T_{stg}	−65 to 150	°C
ESD Protection at any Pin Human Body Model (Note 3)	V_{ESD}	2000	V

1. Either or both inputs should not exceed the range of V_{EE} − 300 mV to V_{EE} + 10 V.
2. Maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded. $T_J = T_A + (P_D R_{\theta JA})$
3. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{CM} = V_O = 0, R_L to GND, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}				mV
V_{CC} = 0.9 V, V_{EE} = −0.9 V					
T_A = 25°C		−7.0	0.6	7.0	
T_A = −40°C to 85°C		−9.0	−	9.0	
V_{CC} = 2.5 V, V_{EE} = −2.5 V					
T_A = 25°C		−7.0	0.6	7.0	
T_A = −40°C to 85°C		−9.0	−	9.0	
V_{CC} = 5.0 V, V_{EE} = −5.0 V					
T_A = 25°C		−7.0	0.6	7.0	
T_A = −40°C to 85°C		−9.0	−	9.0	
Input Offset Voltage Temperature Coefficient (R_S = 50) T_A = −40°C to 105°C	$\Delta V_{IO}/\Delta T$	−	8.0	−	μV/°C
Input Bias Current (V_{CC} = 1.8 V to 10 V)	$\lvert I_{IB} \rvert$	−	1.0	−	pA
Common Mode Input Voltage Range	V_{ICR}	V_{EE}	−	V_{CC}	V
Large Signal Voltage Gain	A_{VOL}				kV/V
V_{CC} = 5.0 V, V_{EE} = −5.0 V					
R_L = 10 kΩ		16	50	−	
R_L = 2.0 kΩ		16	30	−	
Output Voltage Swing, High (V_{ID} = ±0.2 V)	V_{OH}				V
V_{CC} = 0.9 V, V_{EE} = −0.9 V (T_A = 25°C)					
R_L = 10 k		0.85	0.88	−	
R_L = 2.0 k		0.80	0.82	−	
T_A = −40°C to 85°C					
R_L = 10 k		0.85	−	−	
R_L = 2.0 k		0.79	−	−	
V_{CC} = 2.5 V, V_{EE} = −2.5 V (T_A = 25°C)					
R_L = 600		2.10	2.21	−	
R_L = 2.0 k		2.35	2.44	−	
T_A = −40°C to 85°C					
R_L = 600		2.00	−	−	
R_L = 2.0 k		2.40	−	−	
V_{CC} = 5.0 V, V_{EE} = −5.0 V (T_A = 25°C)					
R_L = 600		4.40	4.60	−	
R_L = 2.0 k		4.80	4.88	−	
T_A = −40°C to 85°C					
R_L = 600		4.40	−	−	
R_L = 2.0 k		4.80	−	−	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{CM} = V_O = 0, R_L to GND, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage Swing, Low (V_{ID} = ±0.2 V)	V_{OL}				V
V_{CC} = 0.9 V, V_{EE} = −0.9 V (T_A = 25°C)					
R_L = 10 k		−	−0.88	−0.85	
R_L = 2.0 k		−	−0.82	−0.80	
T_A = −40°C to 85°C					
R_L = 10 k		−	−	−0.85	
R_L = 2.0 k		−	−	−0.78	
V_{CC} = 2.5 V, V_{EE} = −2.5 V (T_A = 25°C)					
R_L = 600		−	−2.22	−2.10	
R_L = 2.0 k		−	−2.38	−2.35	
T_A = −40°C to 85°C					
R_L = 600		−	−	−2.00	
R_L = 2.0 k		−	−	−2.30	
V_{CC} = 5.0 V, V_{EE} = −5.0 V (T_A = 25°C)					
R_L = 600		−	−4.66	−4.40	
R_L = 2.0 k		−	−4.88	−4.80	
T_A = −40°C to 85°C					
R_L = 600		−	−	−4.35	
R_L = 2.0 k		−	−	−4.80	
Common Mode Rejection Ratio	CMRR				dB
V_{in} = 0 to 10 V		65	−	−	
V_{in} = 0 to 5.0 V		60	−	−	
Power Supply Rejection Ratio	PSRR	65	−	−	dB
V_{CC}/V_{EE} = 10 V/Ground, ΔV_S = 2.5 V					
Output Short Circuit Current (V_{in} Diff = ±1.0 V)	I_{SC}				mA
V_{CC} = +0.9 V, V_{EE} = −0.9 V					
Source		−	3.0	−	
Sink		−	−3.0	−	
V_{CC} = +2.5 V, V_{EE} = −2.5 V					
Source		20	25	60	
Sink		−60	−25	−20	
V_{CC} = 5.0 V, V_{EE} = −5.0 V					
Source		50	72	140	
Sink		−140	−72	−50	
Power Supply Current (V_O = 0 V)	I_D				mA
V_{CC} = +0.9 V, V_{EE} = −0.9 V					
T_A = 25°C		−	0.97	1.20	
T_A = −40°C to 85°C		−	−	1.30	
V_{CC} = +2.5 V, V_{EE} = −2.5 V					
T_A = 25°C		−	1.05	1.30	
T_A = −40°C to 85°C		−	−	1.40	
V_{CC} = 5.0 V, V_{EE} = −5.0 V					
T_A = 25°C		−	1.13	1.40	
T_A = −40°C to 85°C		−	−	1.50	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{CM} = V_O = 0, R_L to GND, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_O = −2.0 to 2.0 V, R_L = 2.0 kΩ, A_V = 1.0)	SR	0.7	1.2	3.0	V/μs
Gain Bandwidth Product (V_{CC} = 10 V)	GBW	0.5	1.0	3.0	MHz
Gain Margin (R_L = 10 k, C_L = 5.0 pF)	Am	−	6.5	−	dB
Phase Margin (R_L = 10 k, C_L = 5.0 pF)	ϕm	−	60	−	Deg
Power Bandwidth (V_O = 4.0 Vpp, R_L = 2.0 kΩ, THD ≤ 1.0%)	BW_P	−	130	−	kHz
Total Harmonic Distortion (V_O = 4.0 Vpp, R_L = 2.0 kΩ, A_V = 1.0) f = 1.0 kHz f = 10 kHz	THD	 − −	 0.02 0.2	 − −	%
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	−	>1.0	−	tera Ω
Differential Input Capacitance (V_{CM} = 0 V)	C_{in}	−	2.0	−	pF
Equivalent Input Noise Voltage (Freq = 1.0 kHz)	e_n	−	140	−	nV/√Hz

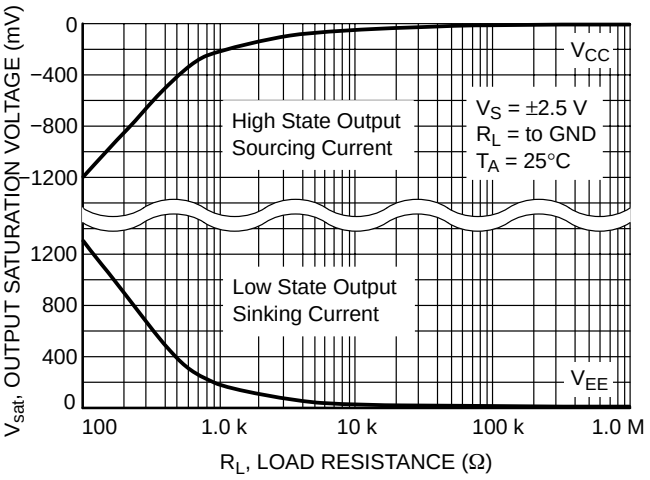


Figure 2. Output Saturation Voltage versus Load Resistance

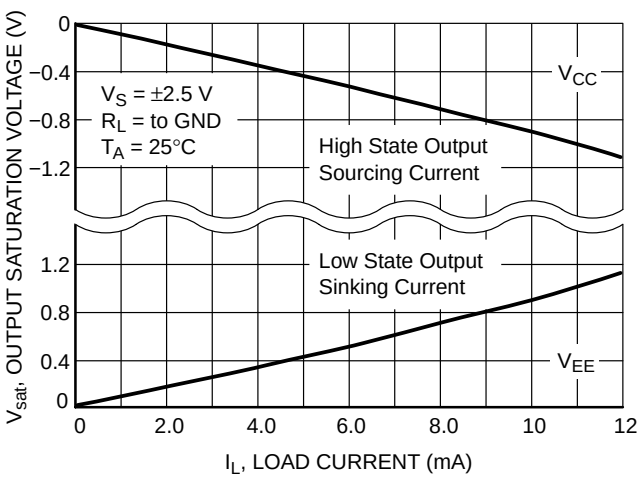


Figure 3. Output Saturation Voltage versus Load Current

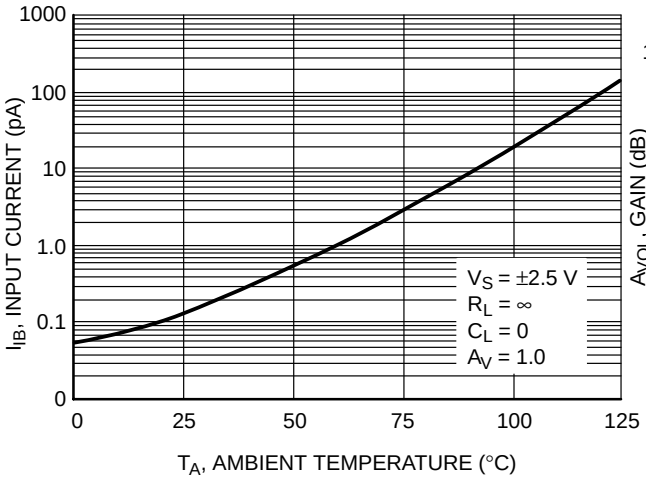


Figure 4. Input Bias Current versus Temperature

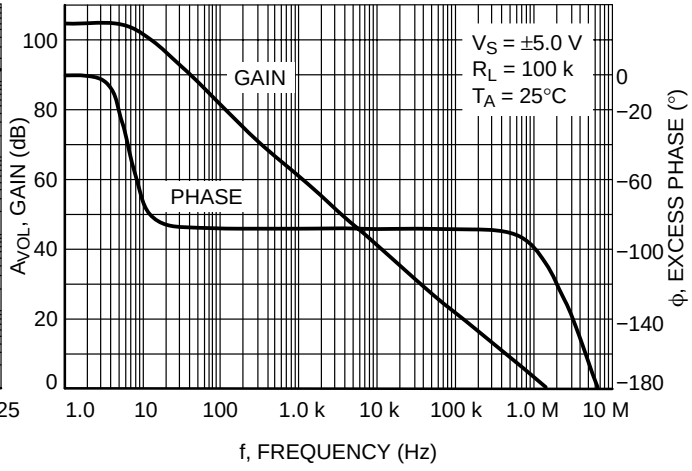


Figure 5. Gain and Phase versus Frequency

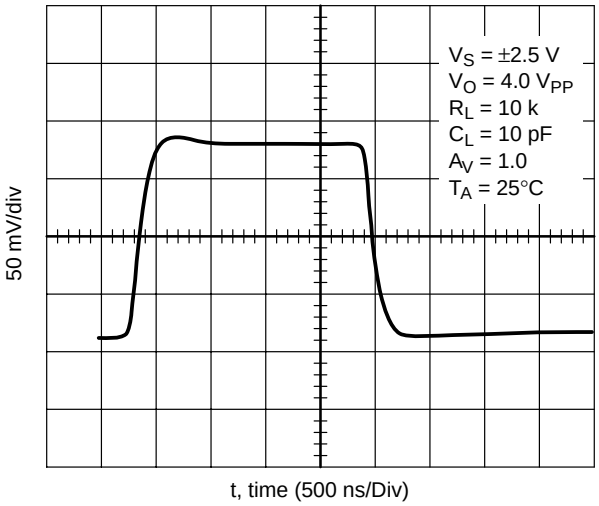


Figure 6. Transient Response

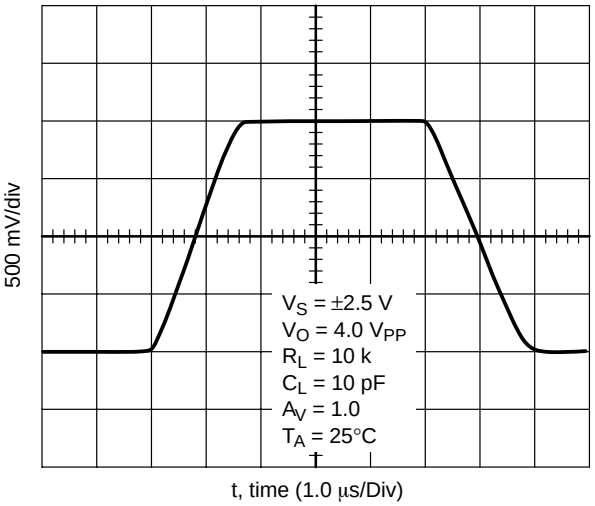


Figure 7. Slew Rate

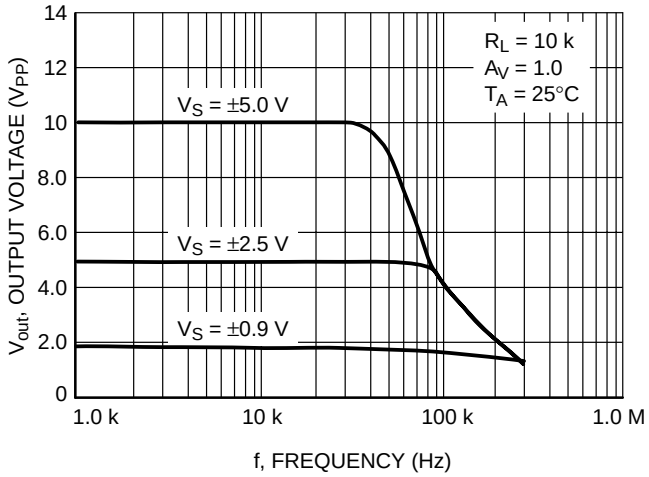


Figure 8. Output Voltage versus Frequency

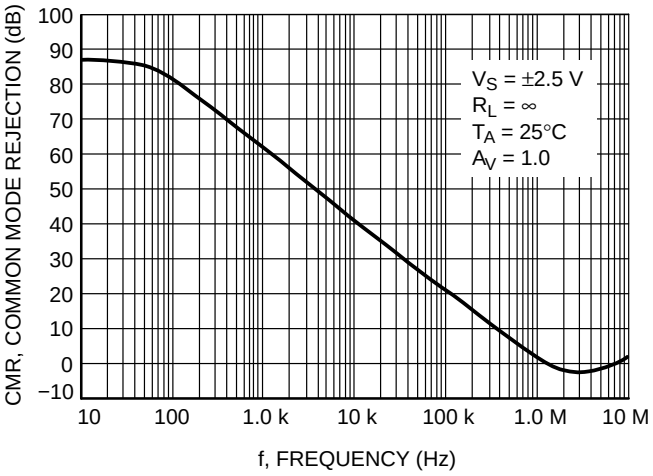


Figure 9. Common Mode Rejection versus Frequency

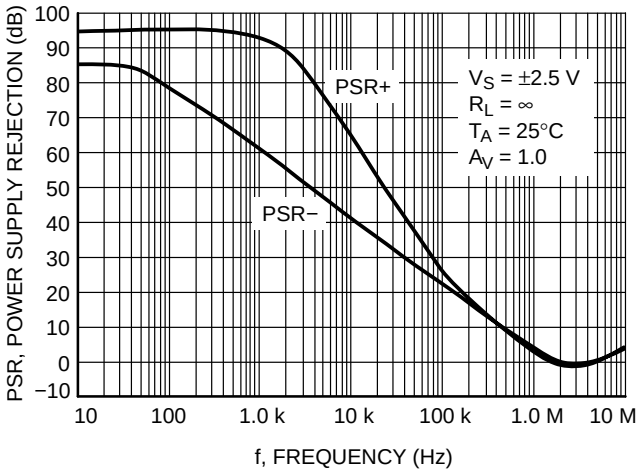


Figure 10. Power Supply Rejection versus Frequency

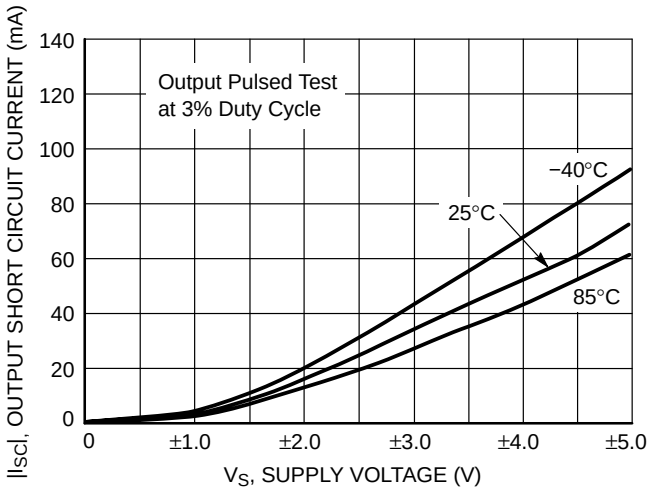


Figure 11. Output Short Circuit Sinking Current versus Supply Voltage

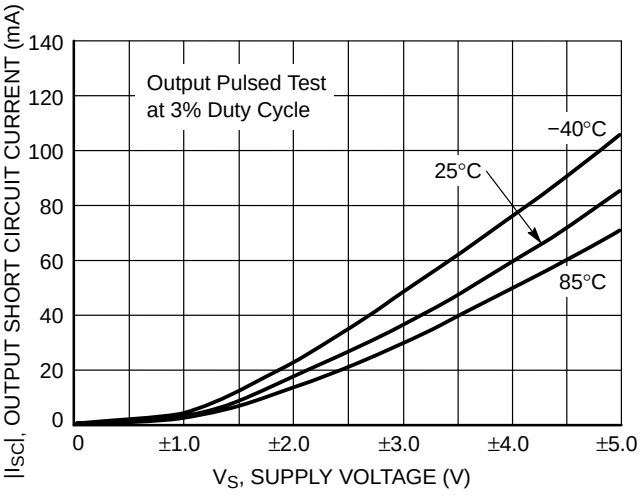


Figure 12. Output Short Circuit Sourcing Current versus Supply Voltage

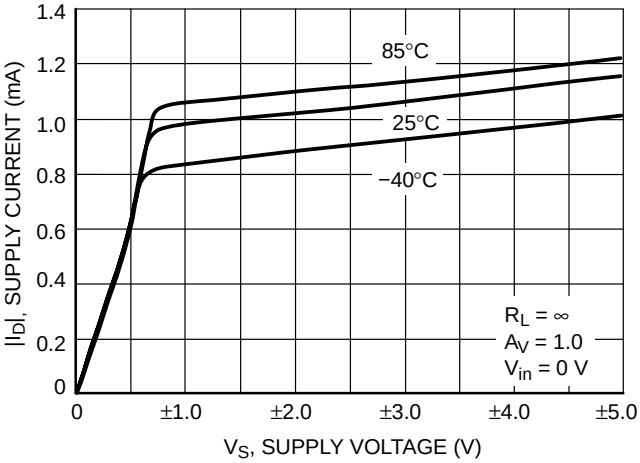


Figure 13. Supply Current versus Supply Voltage with No Load

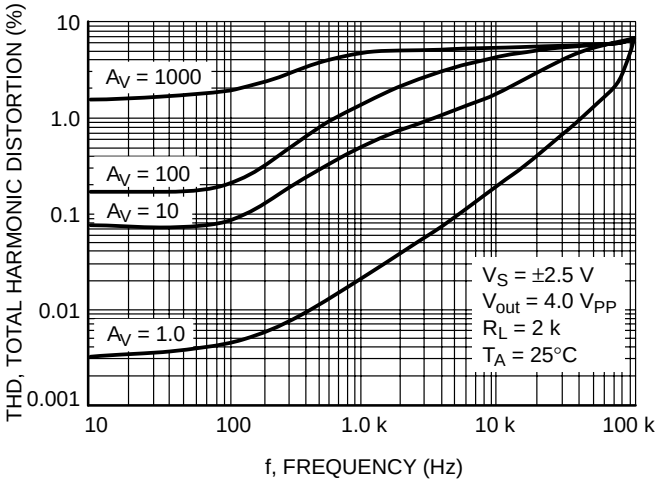


Figure 14. Total Harmonic Distortion versus Frequency with 5.0 V Supply

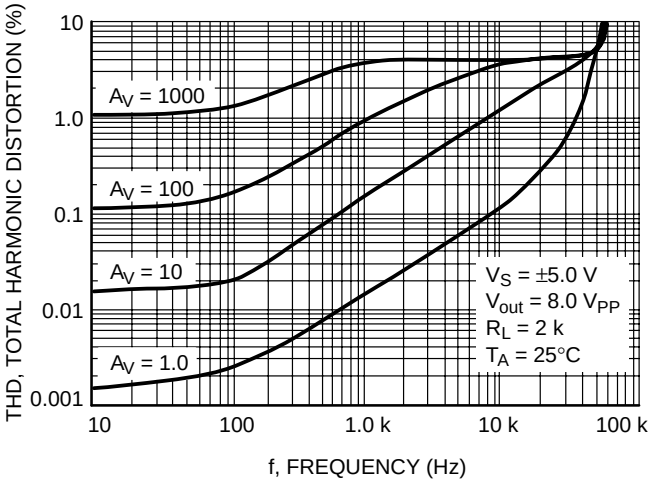


Figure 15. Total Harmonic Distortion versus Frequency with 10 V Supply

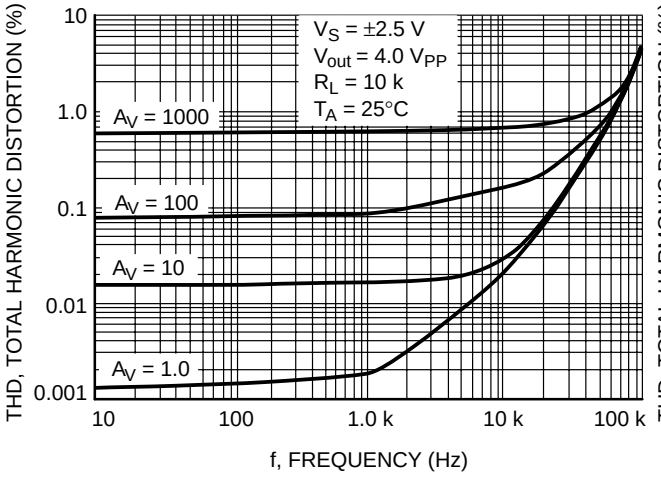


Figure 16. Total Harmonic Distortion versus Frequency with 5.0 V Supply

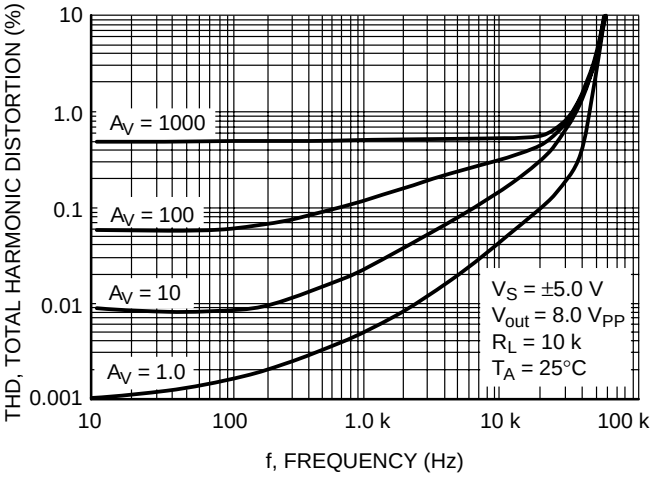


Figure 17. Total Harmonic Distortion versus Frequency with 10 V Supply

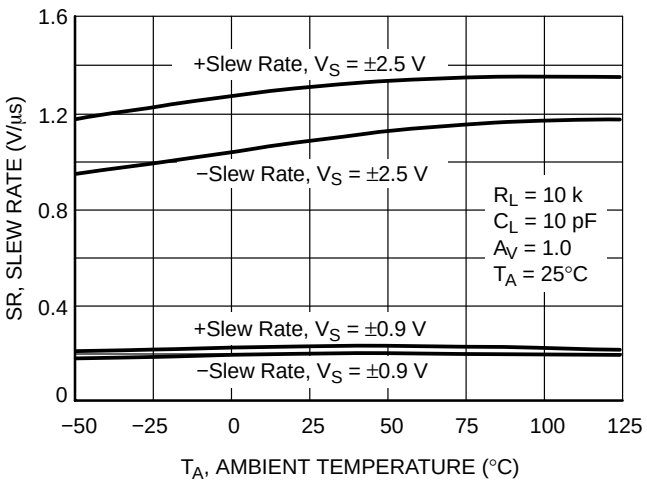


Figure 18. Slew Rate versus Temperature (Avg.)

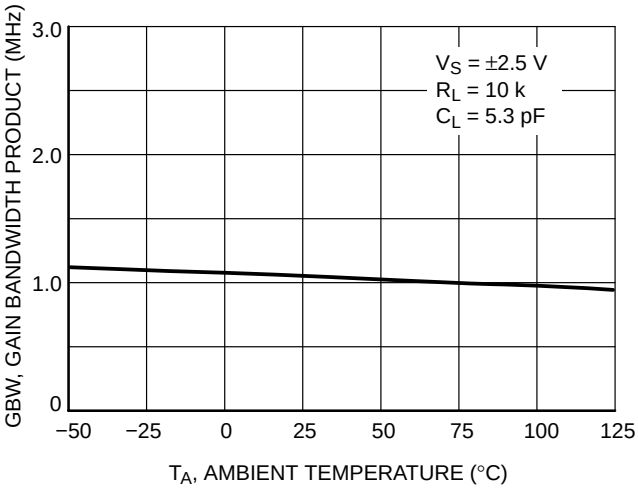


Figure 19. Gain Bandwidth Product versus Temperature

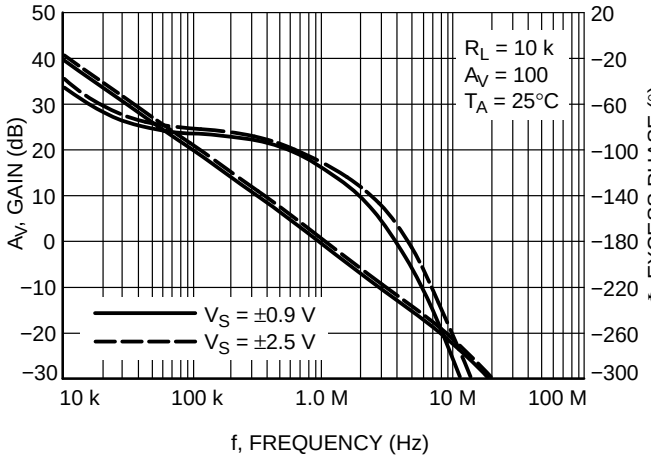


Figure 20. Voltage Gain and Phase versus Frequency

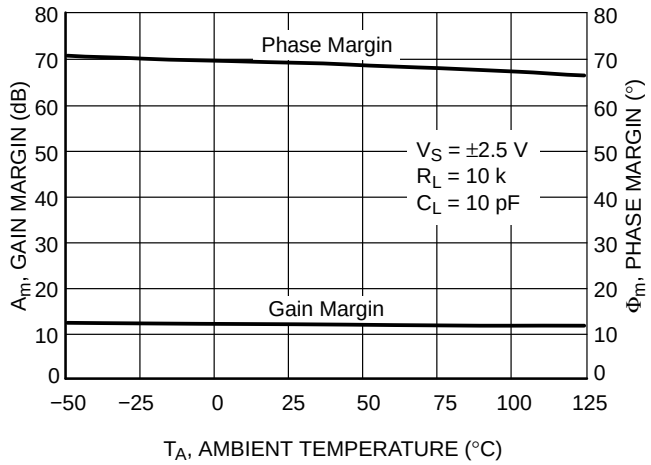


Figure 21. Gain and Phase Margin versus Temperature

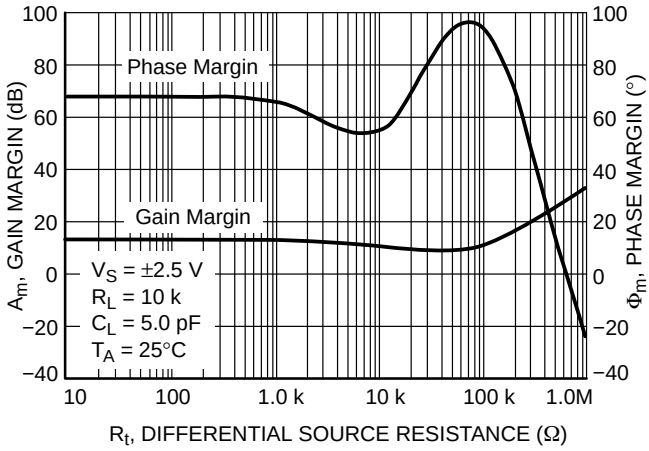


Figure 22. Gain and Phase Margin versus Differential Source Resistance

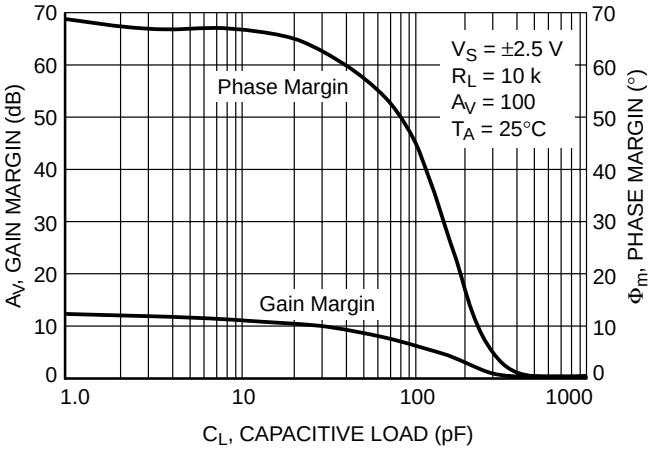


Figure 23. Gain and Phase Margin versus Output Load Capacitance

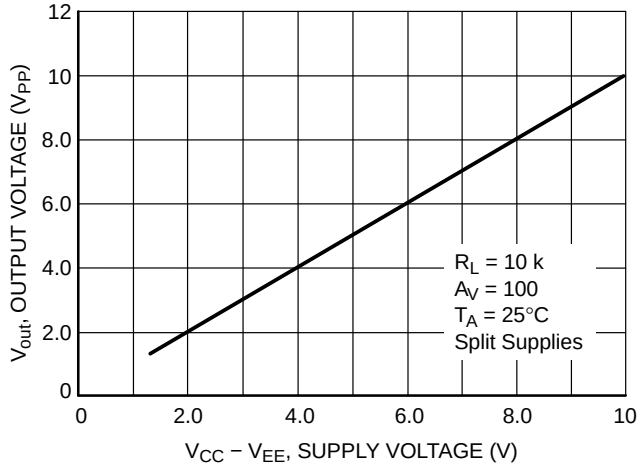


Figure 24. Output Voltage Swing versus Supply Voltage

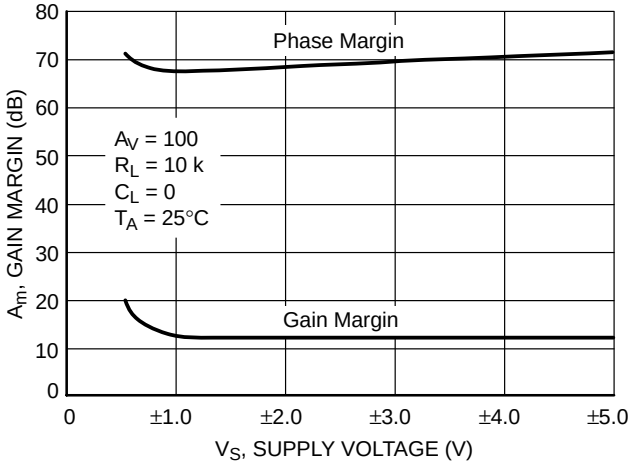


Figure 25. Gain and Phase Margin versus Supply Voltage

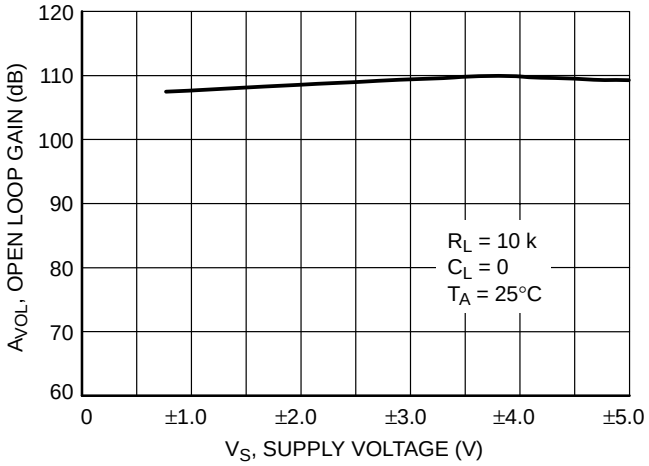


Figure 26. Open Loop Voltage Gain versus Supply Voltage (Split Supplies)

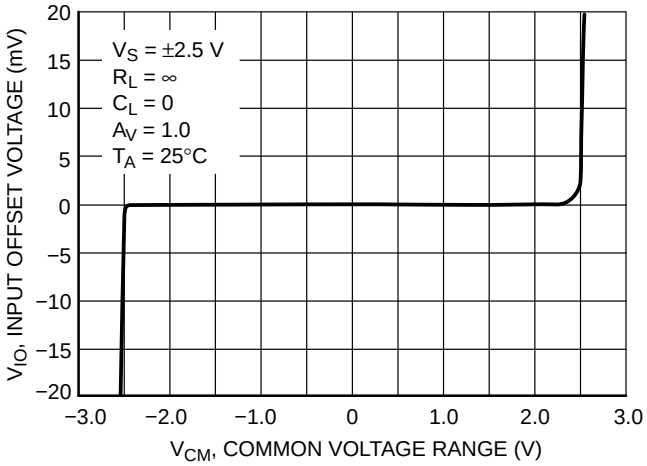


Figure 27. Input Offset Voltage versus Common Mode Input Voltage Range, V_S = ±2.5 V

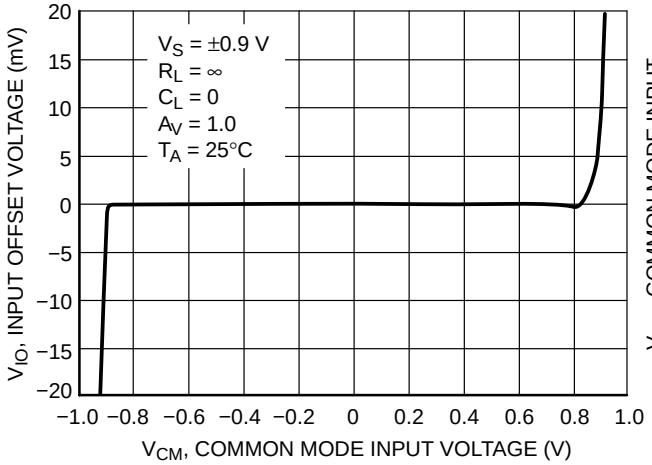


Figure 28. Input Offset Voltage versus Common Mode Input Voltage Range, V_S = ±0.9 V

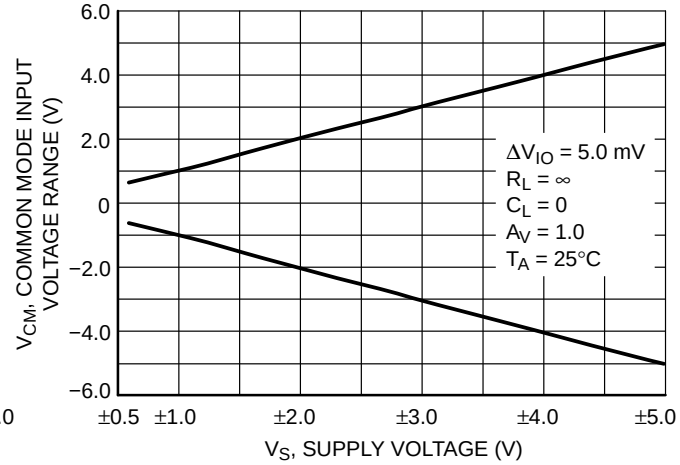


Figure 29. Common−Mode Input Voltage Range versus Power Supply Voltage

APPLICATION INFORMATION AND OPERATING DESCRIPTION

GENERAL INFORMATION

The NCS7101 is a rail−to−rail input, rail−to−rail output operational amplifier that features guaranteed 1.8 volt operation. This feature is achieved with the use of a modified analog CMOS process that allows the implementation of depletion MOSFET devices. The amplifier has a 1.0 MHz gain bandwidth product, 1.2 V/μs slew rate and is operational over a power supply range less than 1.8 V to as high as 10 V.

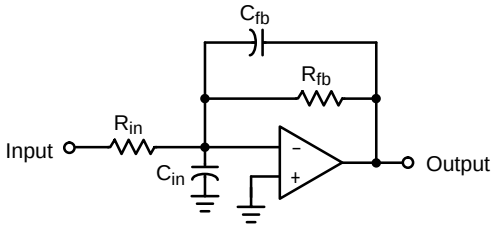
Inputs

The input topology of this device series is unconventional when compared to most low voltage operational amplifiers. It consists of an N−channel depletion mode differential transistor pair that drives a folded cascode stage and current mirror. This configuration extends the input common mode voltage range to encompass the V_{EE} and V_{CC} power supply rails, even when powered from a combined total of less than 1.8 volts. Figures 27 and 28 show the input common mode voltage range versus power supply voltage.

The differential input stage is laser trimmed in order to minimize offset voltage. The N−channel depletion mode MOSFET input stage exhibits an extremely low input bias current of less than 40 pA. The input bias current versus temperature is shown in Figure 4. Either one or both inputs can be biased as low as V_{EE} minus 300 mV to as high as 10 V without causing damage to the device. If the input common mode voltage range is exceeded, the output will not display a phase reversal but it may latch in the appropriate high or low state. The device can then be reset by removing and reapplying power. If the maximum input positive or negative voltage ratings are to be exceeded, a series resistor must be used to limit the input current to less than 2.0 mA.

The ultra low input bias current of the NCS7101 allows the use of extremely high value source and feedback resistor without reducing the amplifier's gain accuracy. These high value resistors, in conjunction with the device input and printed circuit board parasitic capacitances C_{in}, will add an additional pole to the single pole amplifier shown in Figure 30. If low enough in frequency, this additional pole can reduce the phase margin and significantly increase the output settling time. The effects of C_{in}, can be canceled by placing a zero into the feedback loop. This is accomplished with the addition of capacitor C_{fb}. An approximate value for C_{fb} can be calculated by:

$$C_{fb} = \frac{R_{in} \times C_{in}}{R_{fb}}$$



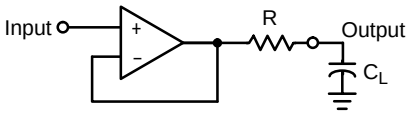
C_{in} = Input and printed circuit board capacitance

Figure 30. Input Capacitance Pole Cancellation

Output

The output stage consists of complimentary P and N channel devices connected to provide rail−to−rail output drive. With a 2.0 k load, the output can swing within 100 mV of either rail. It is also capable of supplying over 95 mA when powered from 10 V and 3.0 mA when powered from 1.8 V.

When connected as a unity gain follower, the NCS7101 can directly drive capacitive loads in excess of 390 pF at room temperature without oscillating but with significantly reduced phase margin. The unity gain follower configuration exhibits the highest bandwidth and is most prone to oscillations when driving a high value capacitive load. The capacitive load in combination with the amplifier's output impedance, creates a phase lag that can result in an under−damped pulse response or a continuous oscillation. Figure 32 shows the effect of driving a large capacitive load in a voltage follower type of setup. When driving capacitive loads exceeding 390 pF, it is recommended to place a low value isolation resistor between the output of the op amp and the load, as shown in Figure 31. The series resistor isolates the capacitive load from the output and enhances the phase margin. Refer to Figure 33. Larger values of R will result in a cleaner output waveform but excessively large values will degrade the large signal rise and fall time and reduce the output's amplitude. Depending upon the capacitor characteristics, the isolation resistor value will typically be between 50 to 500 ohms. The output drive capability for resistive and capacitive loads is shown in Figures 2, 3, and 23.



Isolation resistor R = 50 to 500

Figure 31. Capacitance Load Isolation

Note that the lowest phase margin is observed at cold temperature and low supply voltage.

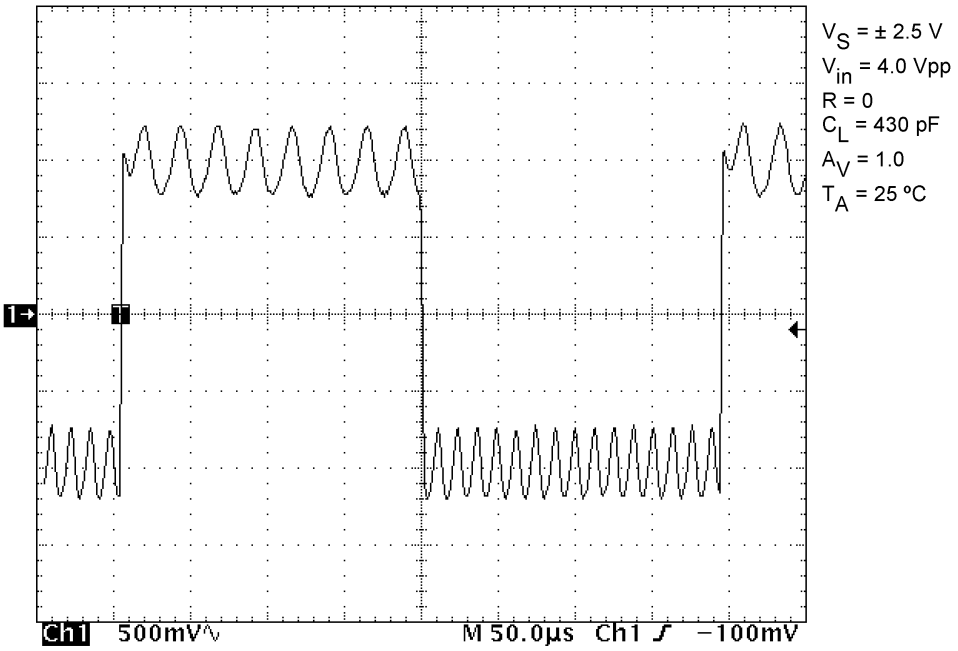


Figure 32. Small Signal Transient Response with Large Capacitive Load

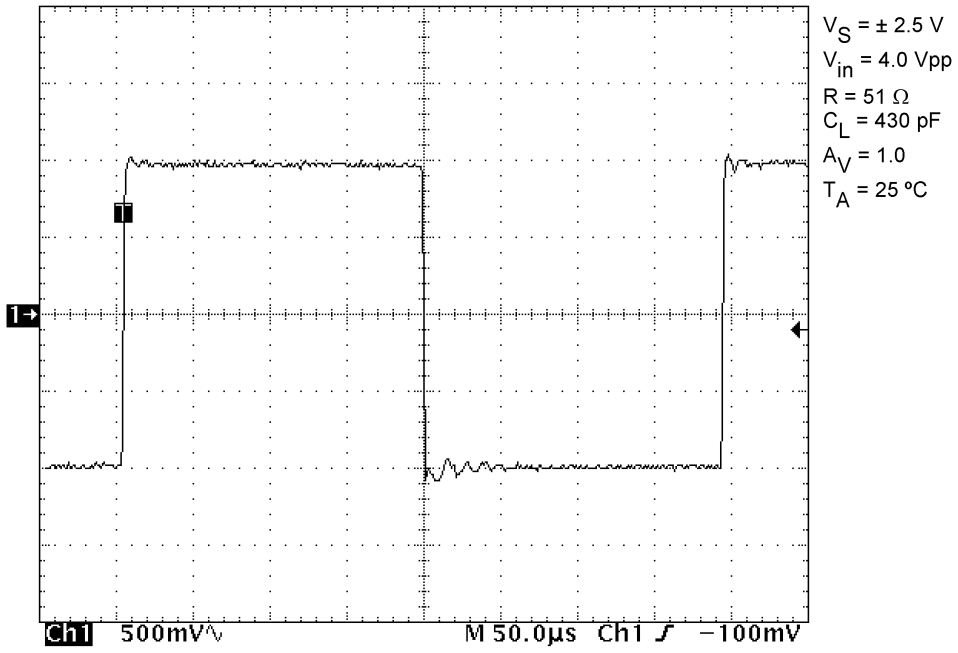
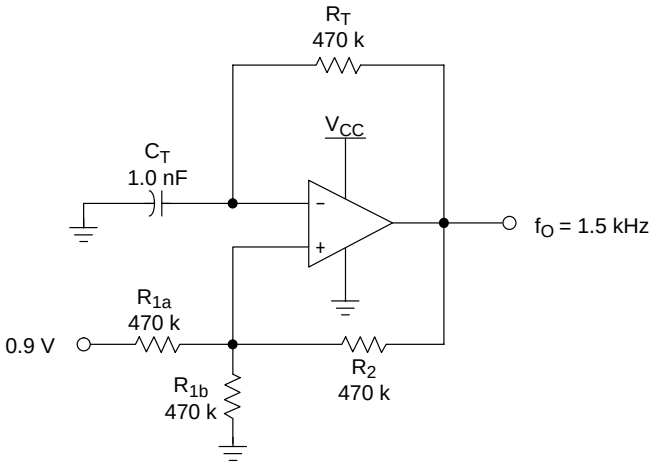
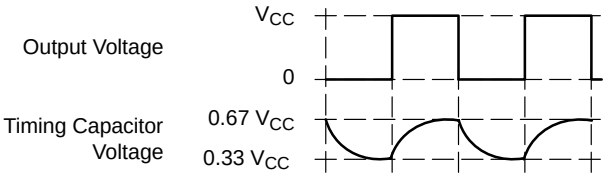


Figure 33. Small Signal Transient Response with Large Capacitive Load and Isolation Resistor.

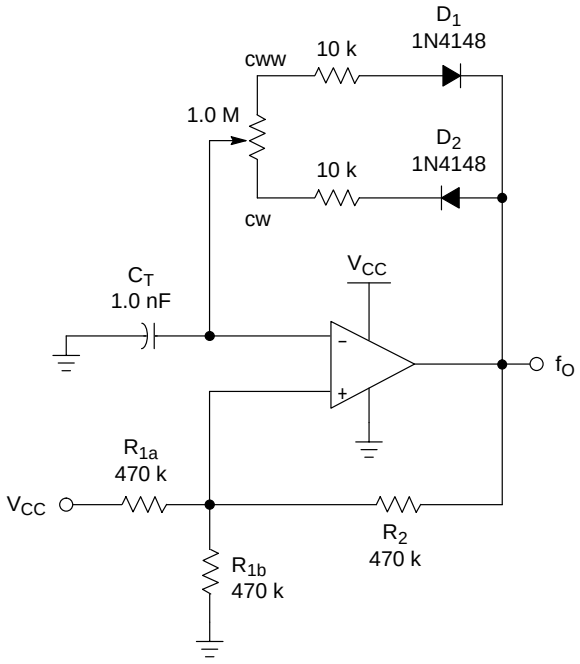


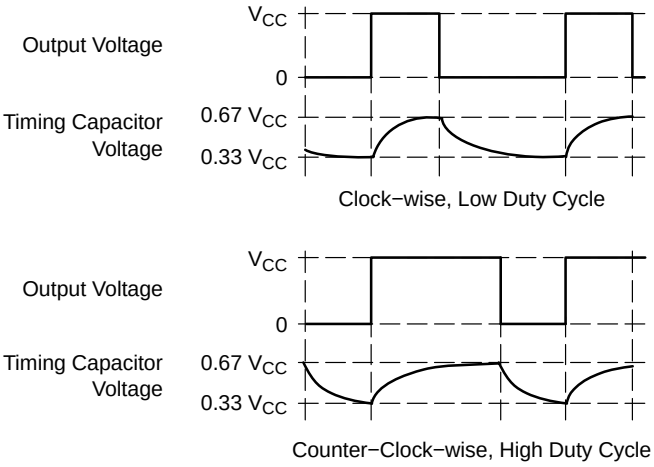


The non−inverting input threshold levels are set so that the capacitor voltage oscillates between 1/3 and 2/3 of V_{CC}. This requires the resistors R_{1a}, R_{1b} and R_2 to be of equal value. The following formula can be used to approximate the output frequency.

$$f_O = \frac{1}{1.39\ R_T C_T}$$

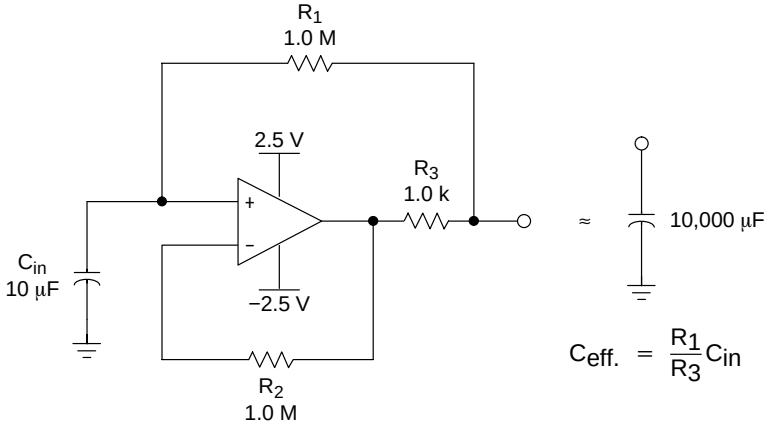
Figure 34. Square Wave Oscillator





The timing capacitor C_T will charge through diode D_2 and discharge through diode D_1, allowing a variable duty cycle. The pulse width of the signal can be programmed by adjusting the value of the trimpot. The capacitor voltage will oscillate between 1/3 and 2/3 of V_{CC}, since all the resistors at the non−inverting input are of equal value.

Figure 35. Variable Duty Cycle Pulse Generator



$$C_{eff.} = \frac{R_1}{R_3} C_{in}$$

Figure 36. Positive Capacitance Multiplier

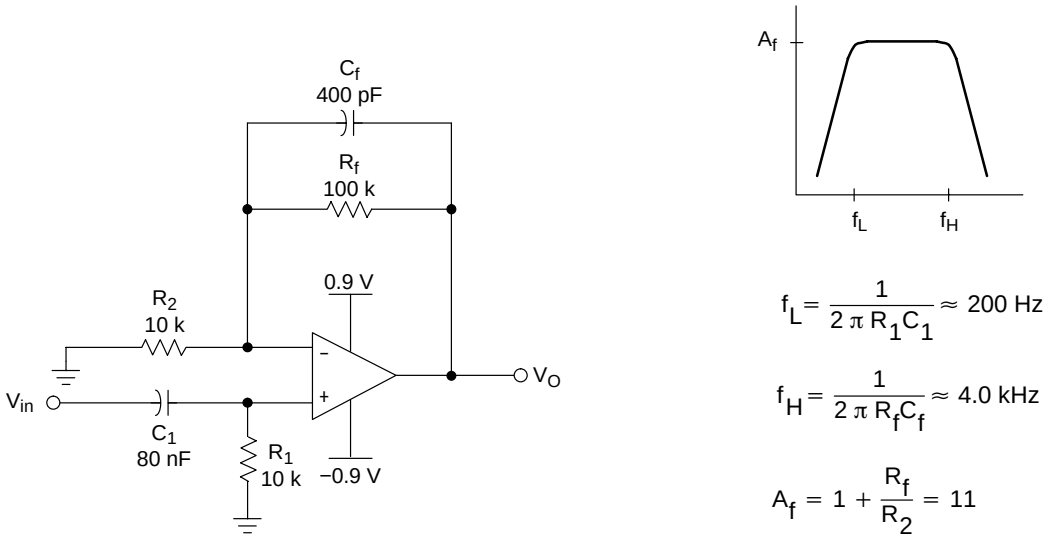


Figure 37. Voice Band Filter

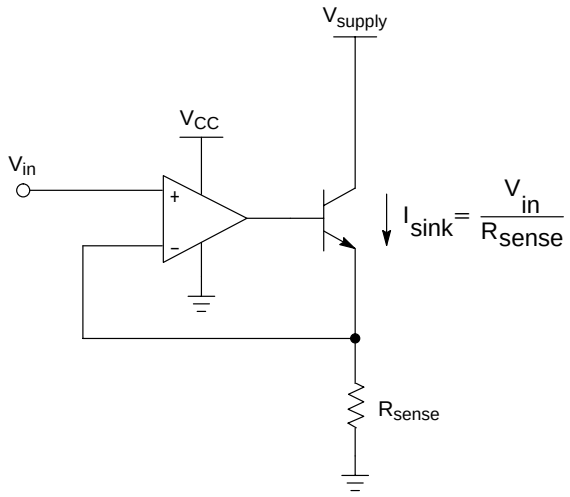
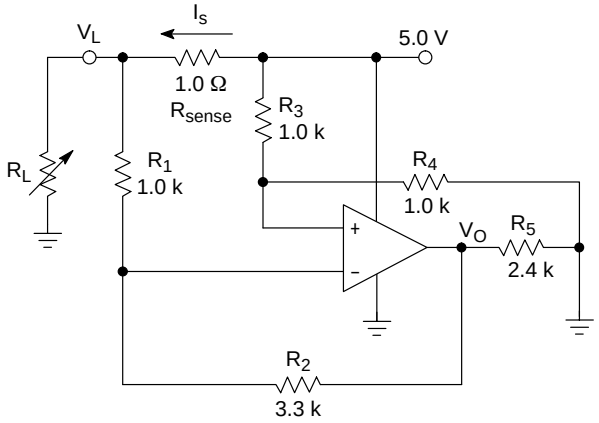


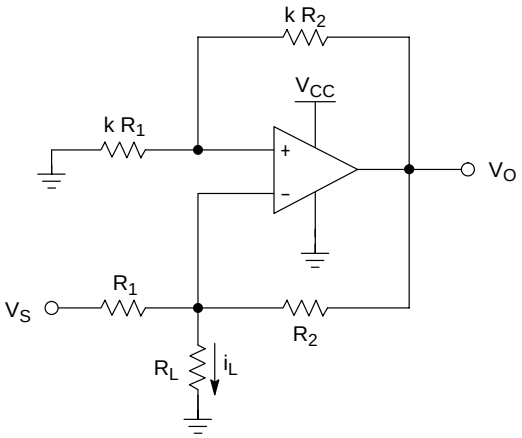
Figure 38. High Compliance Current Sink



I_s	V_O
1.00 A	67.93 mV
0.50 A	78.67 mV

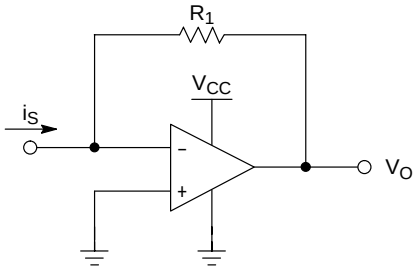
For best performance, use low tolerance resistors.

Figure 39. High Side Current Sense



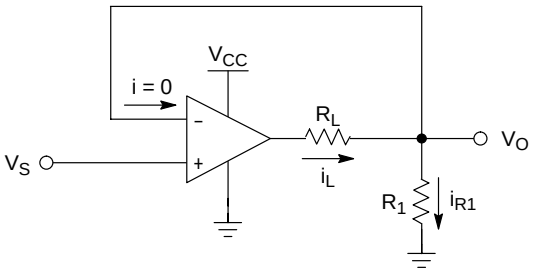
$i_L = \frac{V_S}{R_1}$, Note that i_L is independent of R_L

Figure 40. Current Source



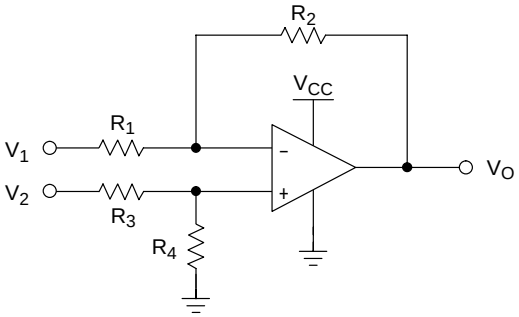
$V_O = -i_S R_1$

Figure 41. Current to Voltage Converter



$i_{R1} = i_L = \frac{V_{R1}}{R_1} = \frac{V_S}{R_1}$

Figure 42. Voltage to Current Converter

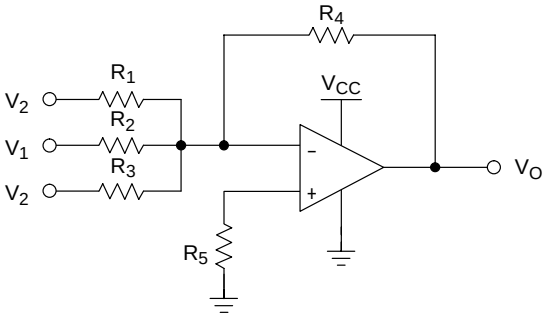


$$V_O = V_2\left[\frac{R_4}{R_3 + R_4}\right]\left[\frac{R_2}{R_1} + 1\right] - V_1\frac{R_2}{R_1}$$

If $R_1 = R_3$, and $R_2 = R_4$, the equation simplifies to:

$$V_O = (V_2 - V_1)\frac{R_2}{R_1}$$

Figure 43. Differential Amplifier



$$V_O = -R_2\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

To minimize input offset current take:
$R_5 = R_1 // R_2 // R_3 // R_4$

Figure 44. Summing Amplifier

PACKAGE DIMENSIONS

SOT−23−5 / TSOP−5, SC59−5
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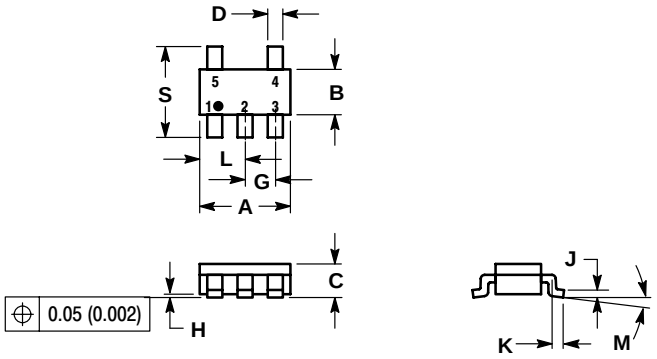
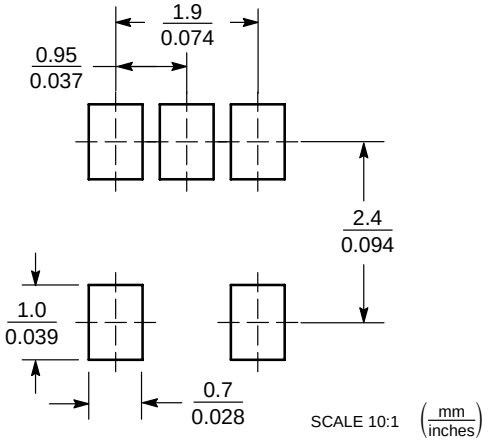


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0	10	0	10
S	2.50	3.00	0.0985	0.1181

SOLDERING FOOTPRINT*



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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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